What is claimed is:

1. A memory trouble relief circuit for relieving the failure of a memory of a semiconductor integrated circuit having the memory, comprising:

a redundancy relief circuit having a redundancy circuit by which the defective part of the memory is replaced based on the diagnosed result of the memory; and

a power line of different system from that of a power source for the semiconductor integrated circuit.

2. A memory trouble relief circuit for relieving the failure of a memory of a semiconductor integrated circuit having the memory, the memory trouble relief circuit comprising:

a self-diagnosis circuit, which diagnoses the memory and outputs the diagnosed result to an external power control circuit and

a redundancy relief circuit, which have a redundancy circuit by which the defective part of the memory is replaced based on the diagnosed result,

wherein the supply of power to the redundancy relief circuit is controlled independently of the supply of power to the semiconductor integrated circuit by the power control circuit operating based on the diagnosed result.

3. A memory trouble relief circuit for relieving the failure of a memory of a semiconductor integrated circuit having the memory, said memory trouble relief circuit comprising:

a holding unit, which for previously holds a diagnosed result of the memory upon inspection of the semiconductor integrated circuit and

a redundancy relief circuit, which have a redundancy circuit by which the defective part of the memory is replaced based on the diagnosed result,

wherein the supply of power to the redundancy relief circuit upon actual use of the semiconductor integrated circuit is controlled independently of the supply of power to the semiconductor integrated circuit by the power control circuit operating based on the diagnosed result.

4. A memory trouble relief circuit according to claim 1, wherein the power to the redundancy relief circuit is supplied from a power source different from that of the semiconductor integrated circuit.

5. A memory trouble relief circuit according to claim 2, wherein the self-diagnosis circuit outputs the diagnosed result of the memory obtained every time the power is turned on to the power control circuit.

6. A memory trouble relief circuit according to claim 1, wherein the replacement of the defective part of the memory is carried out under the control of a fuse.

7. A memory trouble relief circuit according to claim 2, wherein the power control circuit is provided outside the semiconductor integrated circuit.

8. A memory trouble relief circuit according claim 1, wherein the power control circuit is provided inside the semiconductor integrated circuit.

9. A power control method for a memory trouble relief circuit according to claim 1, wherein power is supplied to the redundancy relief circuit only when the defective part of the memory is replaced by the redundancy circuit based on the diagnosed result of the memory.

10. A power wiring method for a memory trouble relief circuit according to claim 1, wherein the power supply line for the redundancy relief circuit is cut by trimming when the defective part of the memory is not replaced by the redundancy circuit based on the diagnosed result of the memory.